JEDEC STANDARD

Gate Charge Test Method

JESD24-2

JANUARY 1991 (Reaffirmed: OCTOBER 2002)

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

Published by

2500 Wilson Boulevard
Arlington, VA 22201-3834

PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications or call Global Engineering Documents, USA and Canada 1-800-854-7179, International (303) 397-7956

Printed in the U.S.A.

PLEASE!

DON'T VIOLATE
THE
LAW!

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

GATE CHARGE TEST METHOD

(From Council Ballot JCB-90-15, formulated under the cognizance of JC-25 Committee on Transistors.)

1. PURPOSE

This method describes a means for measuring the input charge of insulated gate controlled power devices such as Power MOSFETs and IGBTs, N/P type. The text focuses on enhancement-mode field effect transistors.

2. DESCRIPTION

A gate charge test is performed by driving the device gate with a constant current (I_g) and measuring the resulting gate voltage response. Constant gate current scales the gate voltage, a function of time, to a function of coulombs. A small value of gate current is necessary to avoid device and circuit high frequency affects. The slope of the generated response reflects the active device capacitance (C = dq/dvgs) as it varies during the switching transition. Charge or capacitance can be unambiguously specified at any gate voltage.

3. GATE VOLTAGE WAVEFORM

Figure 1 is an idealization of the turn-on gate waveform with a high impedance drain load. Under this condition the turn-off waveform is a mirror image of turn-on. High drain currents require a clamped inductive load or electronic current regulation to maintain high impedance. In these cases gate charge is measured during the turn-off portion of the gate response.

The gate waveform comprises three line segments with slopes S1, S2 and S3. The position and slope of segment 1 is invariant with drain voltage, drain current and junction temperature as is the slope of segment 2. The position of segment 2 is a weak function of drain voltage. The slope of segment 3 is most often very shallow and can be considered zero. The position of segment 3 is determined by the gate plateau voltage, $V_{gs(pl)}$. This voltage is a point on the device transfer curve when $V_{DS} \geq 3\ V_{gs(pl)}$. It is a strong function of drain current and junction temperature.

Q_{gs} and Q_{gd} are gate charges that have been widely published. They may be indirectly determined by performing five measurements and solving the following equations:

$$S1 = (V_2-V_1)/(Q_2-Q_1) = V_{gs(pl)}/Q_{gs}$$

$$S2 = (V_4-V_3)/(Q_4-Q_3) = (V_4-V_{gs(pl)})/[Q_4-(Q_{gs}+Q_{gd})]$$

The third quadrant linear portion of line segment 1 may be used to improve the measurement accuracy of S1.

Low gain devices and/or low impedance drain loads result in a significant departure from the idealization of Figure 1. The slope of line segment 3 is non-zero and is usually accompanied by a lengthy non-linear transition from line segment 1 to line segment 3. Determination of $Q_{gs} + Q_{gd}$ for this condition requires a careful melding of measurement technique and parameter definition as follows:

3. GATE VOLTAGE WAVEFORM (cont'd)

1. $V_{gs(pl)}$ is the gate-source voltage when dv_{gs}/dt first reaches a minimum during device turn-on. During turn-off, the converse is true.

2. S1 should be determined by linear regression using data bounded by $\pm V_{g(th)}$. The correlation coefficient should be 0.9 or greater. Q_{gs} is then determined by:

$$Q_{gs} = V_{gs(pl)}/S1$$

3. The equation of line segment 2 should be determined by linear regression using data bounded by gate voltages that assure the device on-state. The correlation coefficient should be 0.9 or greater. Q_{gd} is then determined by:

$$Q_{gd} = [V_{gs(pl)} - (v_{gs} @ Q = 0)]/S2 - Q_{gs}$$

Figure 3 illustrates the consequences of the aforegoing statements.

3. GATE VOLTAGE WAVEFORM (cont'd)

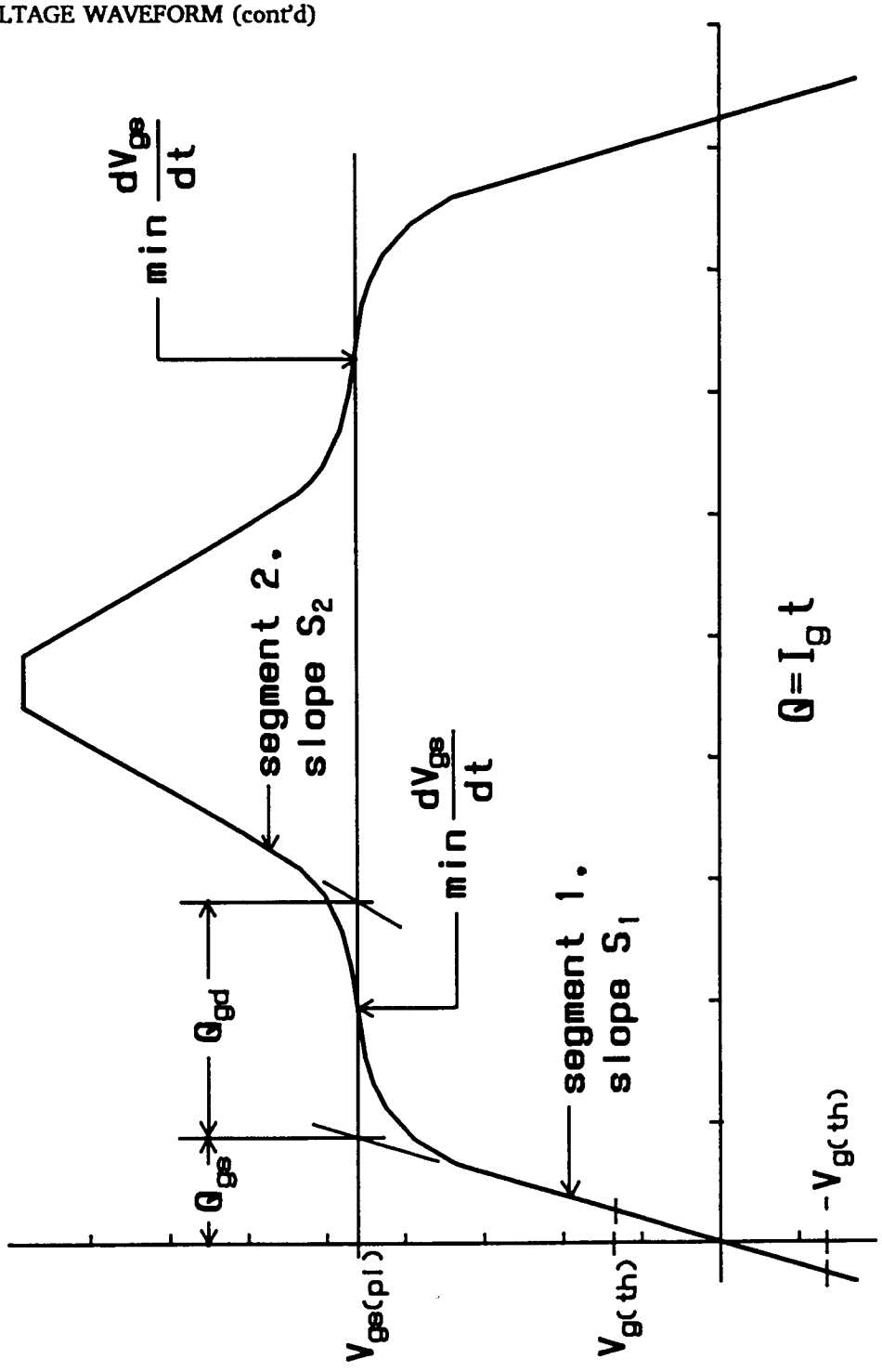

Figure 1
Turn-on Gate Waveform

4. SYMBOLS, TERMS AND DEFINITIONS

$V_{gs(pl)}$ **gate plateau voltage**

The gate-source voltage when dvgs/dt first reaches a minimum during the turn-on switching transition for a constant Ig drive condition. During turn-off it is the gate-source voltage at the last minimum dvgs/dt observed. (Figure 3)

Q_{gs} **gate-source charge**

The gate charge necessary to reach $V_{gs(pl)}$ on the calculated line segment 1. (Figure 1)

Q_{gd} **gate-drain charge ("Miller" charge)**

The gate charge at $V_{gp(pl)}$ on the calculated line segment 2 less Qgs. (Figure 1)

$Q_{g(th)}$ **gate-source threshold charge**

The gate charge necessary to reach a minimum specified gate threshold voltage.

$Q_{g(on)}$ **on-state gate-source charge**

The gate charge necessary to reach a gate-source voltage that will support a minimum specified $I_{D(on)}$.

Q_{gm} **maximum on-state gate-source charge**

The gate charge necessary to reach a specified maximum gate-source voltage.

NOTE: The magnitudes of gate charge and voltage are referred to the coordinate origin (0,0).

5. TEST CIRCUIT

Figure 2 is the generic test circuit. The dynamic response, source impedance and duty factor of the pulsed gate current generator are to be such that they do not materially affect the measurement.

6. REQUIREMENTS

1. T_J - junction temperature.

2. I_D - on-state drain current.

3. V_{DS} - off-state drain voltage.

4. The load impedance should be as high as practical so that the intersection of the three gate charge line segments is reasonably defined when Q_{gs} and Q_{gd} are to be measured. Charge measurements at or below the device threshold voltage are unaffected by load impedance. Measurements in the device on-state ($v_{gs} >> v_{ds}$) are also unaffected by load impedance.

5. I_g - pulsed constant gate current.

6. Gate charge is measured at a specified gate voltage and is referred to the origin (Q_{gd} is the exception).

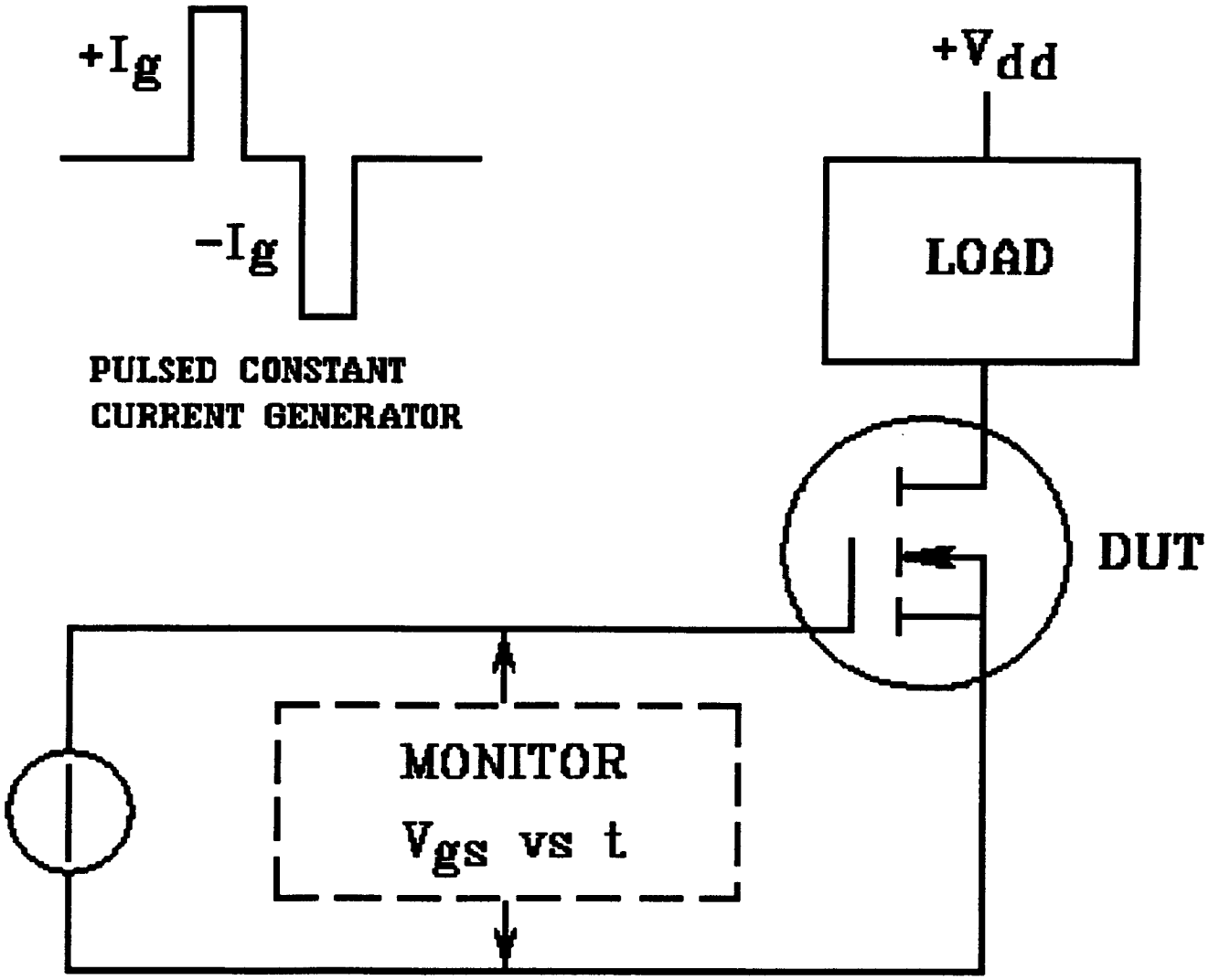

Figure 2
Generic Test Circuit

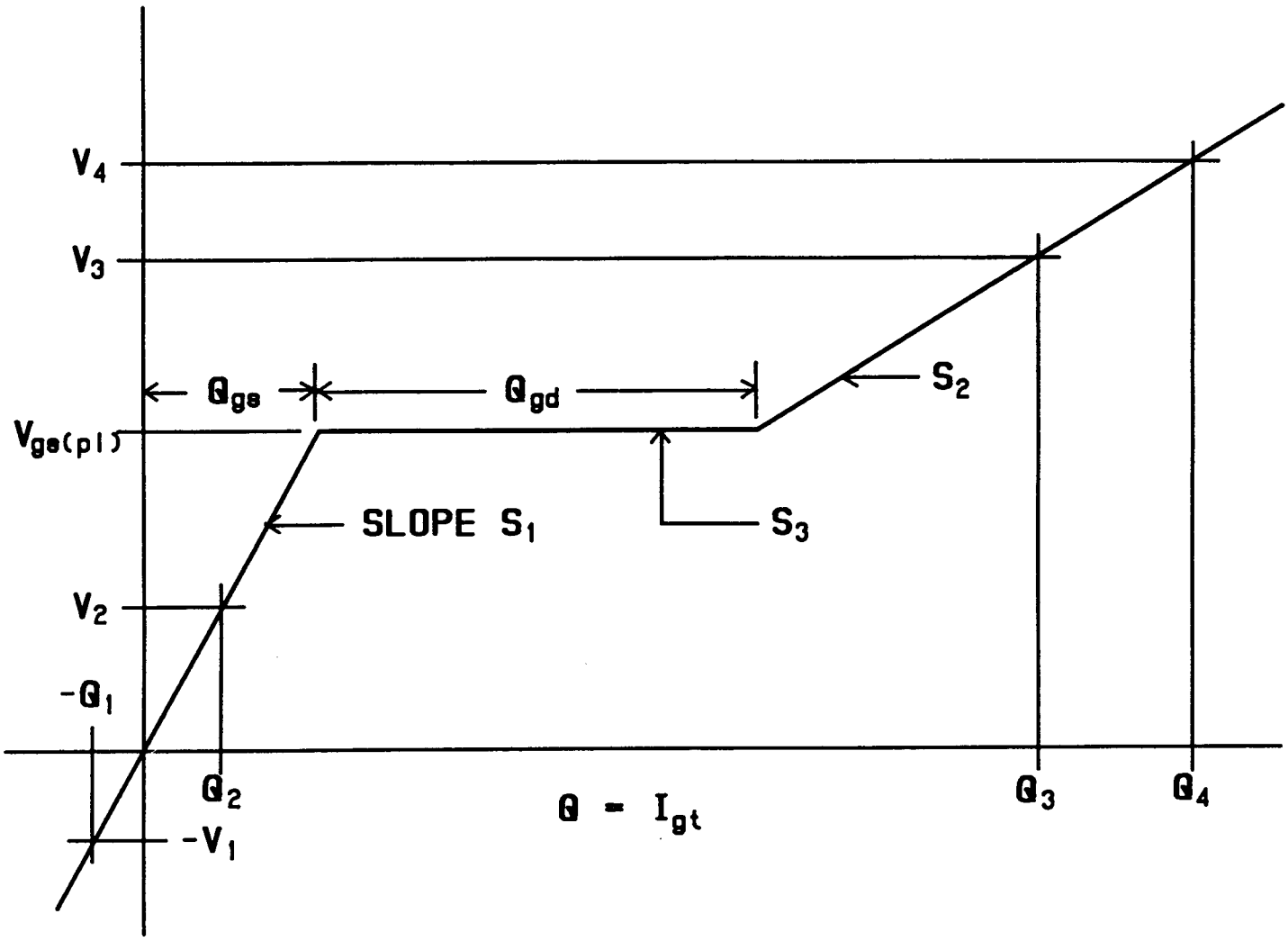

Figure 3
Gate Plateau Voltage


JEDEC